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A Novel Analog Technique Of Generation Of Three Phase SPWM Pulses For Three Phase Inverter

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***Abstract*— Speed controlled electric drives predominately utilise three-phase ac machines. However, since the variable speed ac drives require a power electronic converter for their supply.The DC/AC power converters (inverter) constitute the major unit of the power generation system implemented in Renewable energy sources, AC motor drives and Uninterruptible Power Supply applications. The sinusodial Pulse Width Modulation (SPWM) principle is widely used to control the power switches employed in DC/AC inverters. In this paper, phase locked loop (PLL) base4d simple SPWM generator is presented, which is capable to generate a low-THD, variable voltage variable frequency (VVVF) SPWM pulses synchronized to a pulse input signal that a three decade range of reference frequency from 10 Hz to 200 Hz. The experiment results presented in this paper demonstrate the superiority of the proposed three phase SPWM architecture over its past proposed counterparts based on analog technique in terms of the accuracy of reproducing the desired SPWM pulses.**

Keywords-Voltage controlled oscillator ,switched capacitor filter, phase locked loop, frequency divider, VVVF.

I. INTRODUCTION

Recent advances in fully-controllcd semiconductor switching capability and increases in their power ratings combined with the desire to improve the cfficiency and performance of power electronic systems have been making these enabling technologies a fast-growing field. Nowadays, power electronic technologies influence the design of every system, from office equipment and home appliances to high-speed transportation systems and satellites to name just a few. Applications in both light and heavy industry, such as computer networks, electronic equipment, telecommunications industry, etc. are improved with power electronics support and use [1]. The DC/AC power converters (inverters) are employed in order to transfer the DC energy into the AC, where the objective is to convert the DC input voltage into a sinusoidal AC output voltage of adjustable magnitude and/or frequency. A block diagram of a three phase inverter is shown in Fig. 1. The Sinusoidal Pulse Width Modulation (SPWM) principle is widely used in DC/AC inverters in order to control the operating state of the power switches constituting the DC/AC inverter structure. In this case, the power switches of the converter (e.g. MOSFETs, IGBTs etc.) are set ON or OFF according to the result of the comparison between a high-frequency, constant-amplitude triangular wave (carrier) with three low-variable frequency reference sine-waves of adjustable amplitude. This process is illustrated in Fig. 2. By using the SPWM technique, frequency spectrum of the DC/AC inverter output waveform is formatted such that the non-fundamental harmonic components are located at relatively high frequencies (typically in the order of several kHz). The high-frequency harmonics of the generated SPWM signal, spwm V_o, are then filtered using a low pass LC or LCL type filter, thus producing the high-power and low-frequency sinusoidal waveform V_o, at the DC/AC inverter output terminals (Fig.2). The amplitude of V_o is calculated as follows:

$$V_O = \mathrm{M}.\ \mathrm{E_S} = \frac{Vr}{Vc} \cdot \mathrm{E_S}$$

where E_S (V) is the DC input voltage of the DC/AC inverter, Vr (V) and Vc (V) are the amplitudes of the reference sine and carrier waves, respectively and M is the modulation index. Increasing the frequency of the triangular wave (switching frequency), results in an increase of the DC/AC inverter power density due to the reduction of the volume of the magnetic components comprising the output filter.

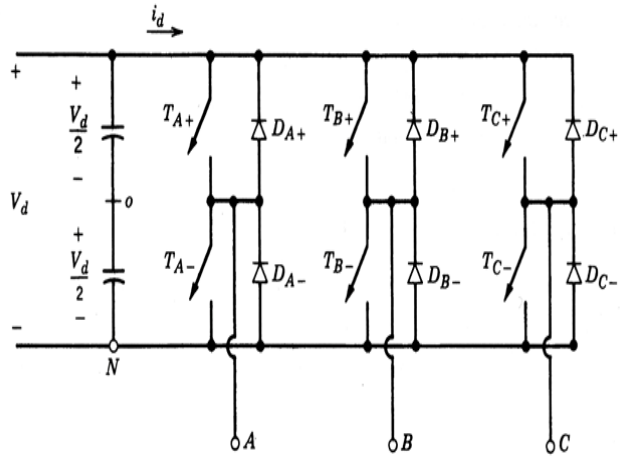

Figure 1. A diagram of DC/AC power converter (inverter)

Different PWM strategies are available in the literature for controlling three phase inverters. The control unit of the DC/AC inverter is used for the execution of control output voltage and it is developed using microcontroller, DSP

and FPGA ICs [2-3], but the complexity appear in there architecture while hardware implementation.

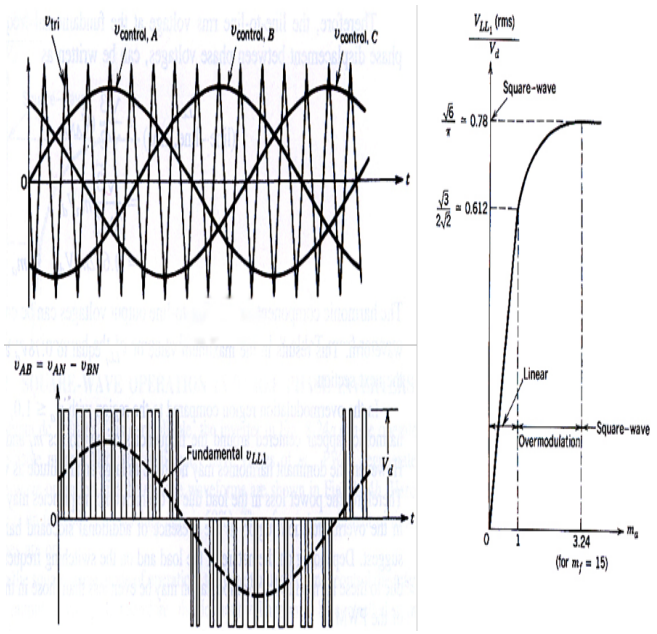

Figure 2.The sinusoidal pulse width modulation principle

In another approach sine wave generation using op-amp analog circuits, shows the decreased in amplitude of sine wave with the increase in frequency. Simple sine wave generation can offer varying degrees of performance but it is difficult to maintain a low THD with constant amplitude if sine wave output must remains locked to a synchronization signal over extended range of frequencies [4]. In the following sections of this paper the architectures of proposed SPWM generation units are analyzed, the proposed Phase locked loop-based SPWM generator is presented and the experimental results are discussed.

II. THE PROPOSED PLL BASED SPWM GENERATOR

The architecture of the proposed PLL-based VVVF SPWM generation unit is illustrated in Fig 3.

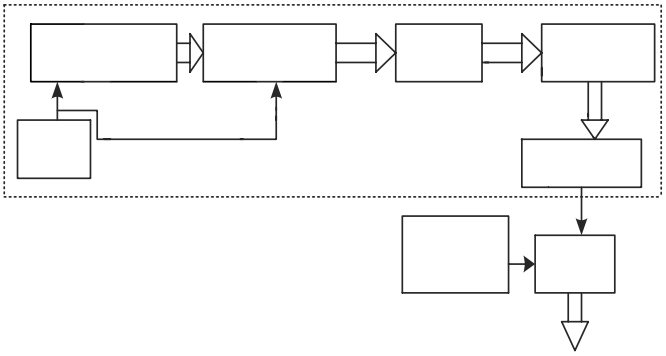

Figure 3.The architecture of the proposed SPWM generator

A. Sine Wave Generating Unit

The sine wave generating uint consists of four major subsystems, which produced variable voltage variable frequency three phase sine wave.

1) Voltage Controlled Oscillator (using 555): A Voltage Controlled Oscillator (VCO) is the synth module that generates the pitch (frequency) of the notes we hear will have both a coarse and fine frequency adjustment knobs. The circuit is sometimes called a voltage–to-frequency converter because the output frequency can be changed by changing the input voltage. In the 555(astable mode) pin 5 terminal is voltage control terminal and its function is to control the threshold and trigger levels. Normally, the control voltage is ++2/3V_{CC} because of the internal voltage divider. However, an external voltage can be applied to this terminal directly or through a pot and by adjusting the pot, control voltage can be varied. Voltage across the timing capacitor is depicted in figure, which varies between +$V_{control}$ and ½ $V_{control}$. If control voltage is increased, the capacitor takes a longer to charge and discharge; the frequency, therefore, decreases. Thus the frequency can be changed by changing the control voltage. Incidentally, the control voltage may be made available through a pot, or it may be output of a transistor circuit, op-amp, or some other device. Like any oscillator, the frequency stays fixed unless something acts on it to change.

$$W=-(R1+R2)*C \ln \frac{Vcc - Vcon}{Vcc - 0.5Vcon}$$

$$T= w + 0.693\ R2\ *C$$

$$F=1/T$$

So that total time period in given by T=W.This circuit is a voltage-controlled oscillator (VCO) that uses the 555 timer IC as the main component. As expected, the 555 timer is configured as an astable multivibrator to be able to serve as an oscillator. An astable multivibrator is just a timing circuit whose output oscillates between 'low' and 'high' continuously, in effect generating a train of pulses.The difference of this circuit with the basic 555 astable circuit is that its 555's pin 5 is tied to an external voltage source. Pin 5 is the 555's control voltage pin, which allows the user to directly adjust the threshold voltages to which the pin 2/pin 6 input voltages are compared by the 555's internal comparators. Since the outputs of these comparators control the internal flip-flop that toggles the output of the 555, adjusting the pin 5 control voltage also adjusts the frequency at which the 555 toggles its output. Increasing the input voltage at pin 5 decreases the output oscillation frequency while decreasing the input voltage increases the output oscillation frequency.

TABLE I: Control voltage Vs. Frequency(For 12 volt V_{CC})

Control voltage (Volts)	Frequency(Hz)
1	1.21kHz
2	1.14kHz

3	994Hz
4.09	857Hz
5.3	739Hz
6.26	636Hz
7.3	540Hz
8.2	494Hz
9	403Hz
10	308Hz
11.3	195Hz
12	61.2Hz

2) Sequential/ Edge trigger unit: The second unit consist of 4017 decade counter IC employs five D flip-flops with master reset capability with the flip-flop being positive-edge-triggered or negative-edge-triggered. It is used to generate three sine wave which are 120° apart from each other. The same control voltage which is used for changing the frequency of voltage controlled oscillator is acts as a supply voltage to this sequential/ Edge trigger unit so that we have to obtained variable voltage variable frequency sine wave.

3) Phase locked loop: The synchronizer IC (74HC4046) is a phase-locked loop (PLL) with one voltage-controlled oscillator (VCO) and three phase/frequency detectors. The best phase/frequency detector to use for maintaining a low THD with constant amplitude is one with a frequency-capture range equal to the VCO frequency range (the maximum frequency minus the minimum frequency). In this case, it is the phase-comparator 2 (PHC 2 out) output.

Phase-locked loop is a feedback loop where a voltage controlled oscillator (VCO) can be automatically synchronized ("locked") to a periodic input signal. The locking property of the PLL has numerous applications in communication systems (such as frequency, amplitude, or phase modulation/demodulation- analog or digital), tone decoding, clock and data recovery, self-tunable filters, and frequency synthesis, motor speed control, etc.

The basic PLL has three components connected in a feedback loop, as shown in the block diagram of Fig 4. A voltage-controlled oscillator (VCO), a phase detector (PD) or phase comparator, and a low-pass loop filter (LPF). The VCO is an oscillator whose frequency *fosc* is proportional to input voltage *vo* (=*Vvcoin*). The voltage at the input of the VCO determines the frequency *fosc* of the periodic signal *vosc* at the output of the VCO. The output of the VCO, *vosc*, and a periodic incoming signal *vi* are inputs to the phase detector. When the loop is locked on the incoming signal *vi*, the frequency *fosc* of the VCO output *vosc* is exactly equal to the frequency *fi* of the periodic signal *vi*, *fosc* = *fi* (1) It is also said that the PLL is in the locked condition. The phase detector produces a signal proportional to the phase difference between the incoming signal and the VCO output signal. The output of the phase detector is filtered by a low-pass loop filter. The loop is closed by connecting the filter output to the input of the VCO. Therefore, the filter output voltage *vo* controls the frequency of the VCO.

A basic property of the PLL is that it attempts to maintain the frequency lock (*fosc* = *fi*) between *vosc* and *vi* even if the frequency *fi* of the incoming signal varies in time. Suppose that the PLL is in a locked condition, and the frequency *fi* of the incoming signal increases slightly. The phase difference between the VCO signal and the incoming signal will begin to increase in time. As a result, the filter output voltage *vo* increases, and the VCO output frequency *fosc* increases until it matches *fi*, thus keeping the PLL in a locked condition. The range of frequencies from *fi* = *fmin* to *fi* = *fmax* where the locked PLL remains in the locked condition is called the ***lock range*** of the PLL. If the PLL is initially locked, and *fi* becomes smaller than *fmin*, or if *fi* exceeds *fmax*, the PLL fails to keep *fosc* equal to *fi*, and the PLL becomes unlocked, *fosc* ≠ *fi*. When the PLL is unlocked, the VCO oscillates at the frequency *fo* called the centre frequency, or the free-running frequency of the VCO. The lock can be established again if the incoming signal frequency *fi* gets close enough to *fo*. The range of frequencies *fi* = *fo* – *fc* to *fi* = *fo* + *fc* such that the initially unlocked PLL becomes locked is called the ***capture range*** of the PLL.

The lock range is wider than the capture range. So, if the VCO output frequency *fosc* is plotted against the incoming frequency *fi*, we obtain the PLL steady-state characteristic shown in Fig. 5. The characteristic simply shows that *fosc* = *fi* in the locked condition, and that *fosc* = *fo* = *constant* when the PLL is out-of-locked (unlocked). A hysteresis can be observed in the *fosc* (*fi*) characteristic because the capture range is smaller than the lock range.

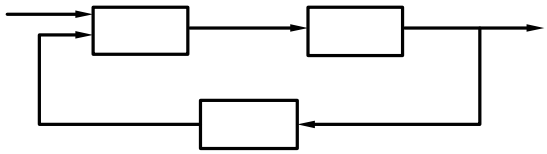

Figure 4. Block diagram of basic phase locked loop

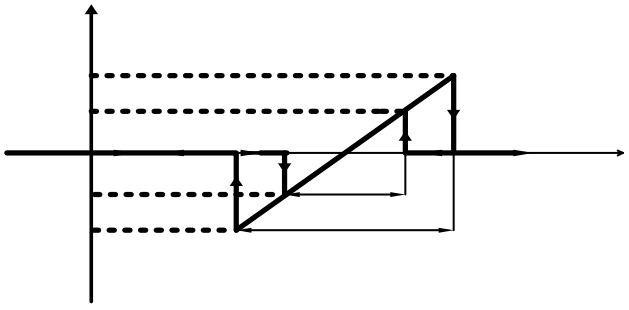

Figure 5. Characteristic of phase locked loop

4) Switched-Capacitor Low-Pass Filter: The MAX297 switched-capacitor low-pass filter that follows the PLL has a cutoff frequency (from analog signal input to analog output)

equal to 1/50th of the frequency at its clock input. Any signal with a ratio to the clock frequency lower than 50 is heavily attenuated.That clock signal is, in this case, the VCO output.The response of filter is shown in fig 6.

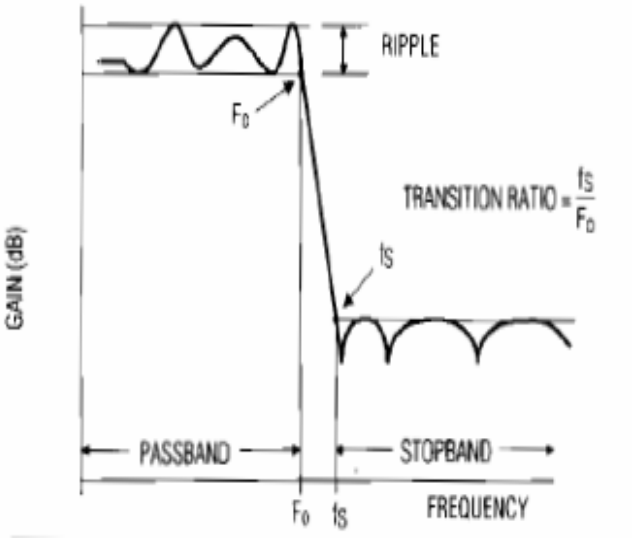

Figure 6: Elliptical Filter Response

No other harmonic component of the input square wave will fall within this band pass, because the ratio of the clock frequency to frequency is always less than 50. The fact that the filter's analog input signal is a 50% duty cycle square wave helps in this application because such a square wave contains only odd harmonics of the fundamental. The lowest frequency harmonic is then the third, which is well within the filter's deep attenuation range (frequency to clock ratio is 21.33 for the 3rd harmonic).

B. Triangular Wave generating Unit

In order to generate a triangular wave, a 555 astable timer and opamp as a inverter is used. Instead of generating bipolar triangular wave, two unipolar triangular wave is generated, one is of positive and other is of negative going triangular wave. The triangular wave is of high frequency i.e. above 20KHz.

C. Triangular- Sine Comparision (Comparator Unit)

The generation of the Pulse Wave Modulation is obtained comparing the triangular wave with the sine. Since we have to control a three-phase inverter, we need to generate complementary PWM signal for each of the three legs. The six switching SPWM pulses for turning on of six switches is generated using comparator.

III. EXPERIMENTAL INVESTIGATION

Experimental investigation is performed to implement the proposed VVVF SPWM strategies for a three phase inverter. PWM output is generated by the comparator units.The experimental waveforms for sinusoidal output are illustrated in Fig.7. for 50 Hz fundamental output and fig 8. shows carrier triangular waveform of 20kHz frequency.

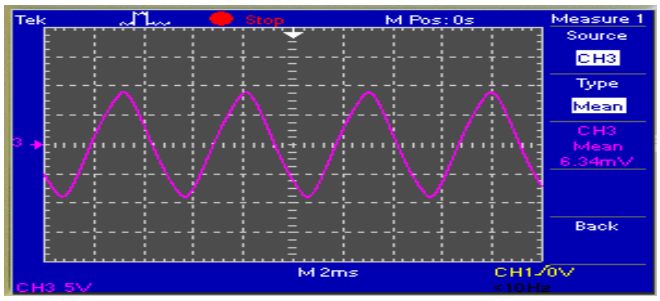

Figure 7: Reference Sine Wave of 50 Hz frequency

THD and amplitude vs. frequency of the proposed reference sine wave generation is illustrated in the table 2. which shows amplitude of sine wave is increases with the increase in the frequency.

TABLE II: THD and amplitude vs. frequency

Frequency(Hz)	THD (%)	Amplitude(VRMS)
10	2.775	1
30	2.650	1.7
50	2.525	3
70	2.250	4
90	1.002	5.1
110	0.986	6.74
130	0.760	7.7
150	0.530	8.91
165	0.405	10
190	0.405	11
200	0.403	12

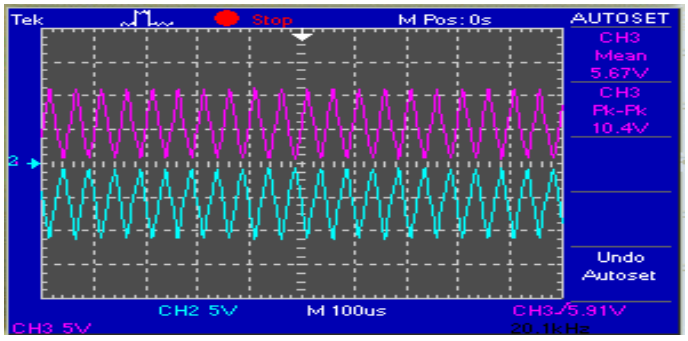

Figure 8: Carrier Triangular Wave of 20 Khz frequency

The gating signals for turning on the switches are generated by comparing a high frequency carrier signal with a sinusoidal reference signal of desired frequency and it is shown in fig 9. It is generated by comparing 20 KHz carrier wave and 50 Hz reference sine wave.

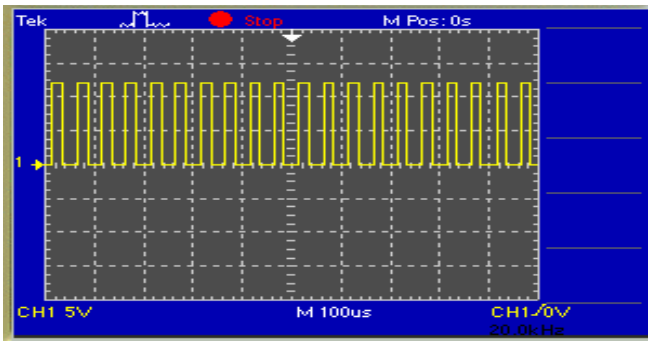

Figure 9: SPWM pulses

IV. CONCLUSION

The SPWM principle is widely used to control the operation of power electronic DC/AC converters. The experimental results presented in this paper verify that the maximum operating reference frequency. In this paper, an PLL based SPWM generator has been presented, which is capable to operate at switching frequencies up to 20 KHz, thus it is capable to support the high switching frequency requirements of modern power electronic DC/AC converters.

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