PERFORMANCE ANALYSIS OF FLASH ANALOG TO DIGITAL CONVERTER WITH TRACK AND HOLD CIRCUIT USING CADENCE PSPICE

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Abstract **-** *This paper proposes a new low power design technique for high speed flash analog to digital converters. This low power design technique will reduce the power consumption of flash A/D converters by 50% reduction of the number of comparators in the circuit. The outputs from the comparators are in thermometer code, an encoder is used to convert this thermometer code to binary code. A novel track and hold circuit which is introduced in this technique. The flash A/D converter using the proposed T/H circuit can realize the same accuracy with the conventional one. Its power consumption is evaluated by CADENCE PSPICE simulations. It is confirmed that the proposed technique can save 35% of power consumption compared with the conventional one.*

KEY WORDS:

Flash Analog/Digital Converters, comparator, Track and Hold Circuit, Thermometer to binary encoder, CADENCE, PSPICE.

I.INTRODUCTION:

Very high speed A/D converters are the important integral part of wireless communication systems. To realize very high speed analog to digital converters, Flash analog to converters are the standard approach [1]. Figure 1 shows a basic circuit diagram of a 3-bit flash A/D converter. This circuit diagram consists of a track and holds circuit, a row of resistors, comparators and following digital circuits. T/H circuits are necessary to prevent an error caused by clock skew especially for high speed A/D converters [2]. T/H circuits keep their output voltage while comparators decide their output voltage level. A row of resistors connected to *Vmax* and *Vmin* creates reference voltages where *Vmax* and *Vmin* are upper and lower limit of the input range of the A/D converter respectively. $2^N - 1$ comparators are used in an *N*-bit flash converter and a sampled input signal is fed parallel to $2^N - 1$ comparators. The comparators compare the input signal and the reference voltages simultaneously. They convert the input signal in to a thermometer code. A time required for the conversion is ideally only one clock cycle. The

thermometer code is decoded into *N*-bit binary code easily by using an encoder circuit.

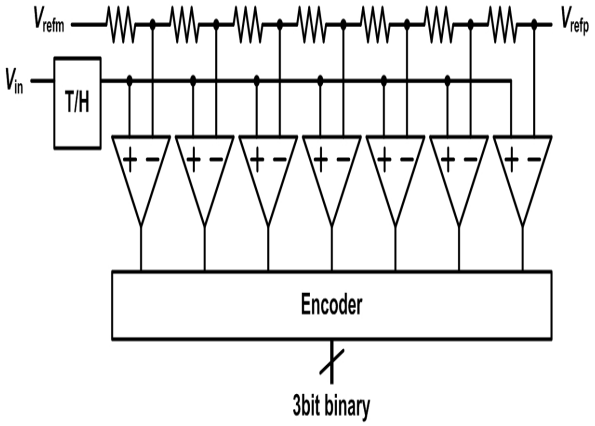

Fig.1 Flash A/D converter for 3-bits.

According to speed, Flash A/D converters are very fast, but they require a large number of comparators, which will occupy a large chip area and very high power consumption. Especially their power consumption becomes larger and larger as their clock frequency becomes higher. The power consumption of output buffers of the T/H circuits followed by the comparators also becomes large to charge and discharge the large input capacitance of $2^N - 1$ comparators quickly. Therefore, reducing the power consumption of flash A/D converters becomes one of the most important issue for high speed analog to digital conversion. Reduction of the number of comparators is particularly effective for low-power operation [6]. This paper proposes a low-power design technique for a flash A/D converter by using the proposed Track/Hold circuit.

II.PROPOSED LOW POWER TECHNIQUE:

The Analog to digital converter is the key component in modern electronic systems. As the digital signal processing industry grows, the ADC design becomes more and more challenging for researchers. Nowadays ADC becomes a part of the system on chip instead of standalone circuits for data converters. This increases the requirements on ADC design concerning for example speed, power, area, resolution, noise etc.New techniques and methods are going to develop day by day to achieve high performance ADCs, Among all types of ADCs, the flash ADC is not only famous for its data conversion rate but also it becomes the part of other types of ADCs for example pipeline and sigma delta ADCs.The main problem with flash ADC is its power consumption. The performance limiting blocks in flash ADCs are comparators.

By using balanced signals, the common mode noise in analog circuits will be suppressed. The comparators whose reference voltages are around the input signal are significant and the other comparators are removed for the simulation purpose. Hernce the power consumption is reduced.

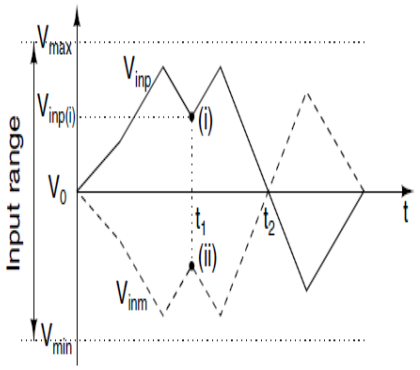

Fig.2.Balanced input signals of Flash A/D Converters.

Therefore in this paper balanced input signals as shown in figure 2. are used as input signals for the flash A/D converters.

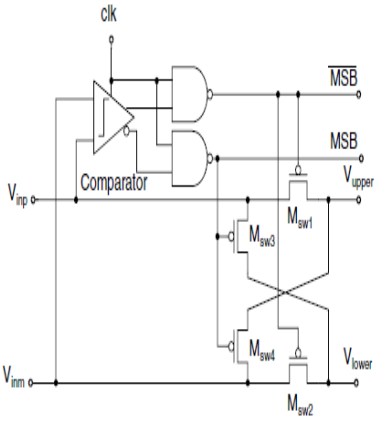

Fig.3.Track and Hold circuit

A T/H circuit shown in Fig.3 is used in the first stage of the A/D converter[4]. The T/H circuit consists of four MOSFET switches realized by the clock signal and the output voltage of a comparator which compares two input signals are applied to NAND gates and their output voltages are used to drive these MOSFET switches. From MOSFET switches, two output voltages named Vupper and Vlower are obtained. These two signals are the input signals for the comparator circuit and the 4 to 2 encoder circuit.

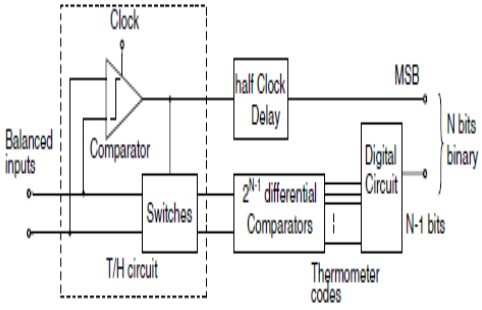

Fig.4.Block diagram of the proposed A/D Converter.

A block diagram of a flash A/D converter based on the proposed technique is shown in Fig. 4.When *Vinp* is in the upper half of the input range switches realized by M*sw*1 and M*sw*2 are turned on. When *Vinp* is in the lower half of input range M*sw*3 and M*sw*4 are shorted to exchange the input signals. When clock signal is low, all of switches are opened and the output voltage is kept constant. During this term, the following comparators evaluate the input signals. The output voltage of one of NAND gates are also used as the MSB of the A/D converter [9].

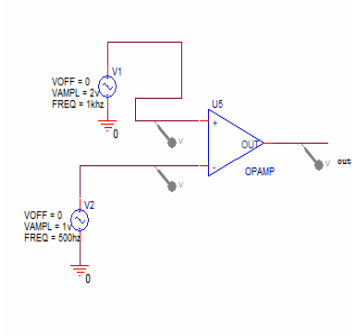

Fig.5.comparator

A comparator shown in Fig. 5 is used in Fig. 4. The proposed 3-bit flash A/D converter shown in Fig. 4 is realized by using CADENCE spice tool. Therefore only $2^{N-1}+1$ comparators are required for the proposed flash A/D converter where extra one comparator is used in the T/H circuit.

The above discussion is based on an identical condition which the common mode voltage of two input signals is assumed to be equal to the middle of input range[10]. When the input signals have offset voltages one of input signals might be out of input range of the upper or lower half of comparators and it might cause an error. The input range of the comparators is designed to be lapped over in actual design to prevent this error.

IV. SIMULATION RESULTS

A. Comparator Output Waveform

As shown in fig.5 sine wave signal is applied to the non inverting terminal of the comparator and reference signal is applied to the inverting terminal of the comparator. We have got the following simulation waveform as shown in fig.6.

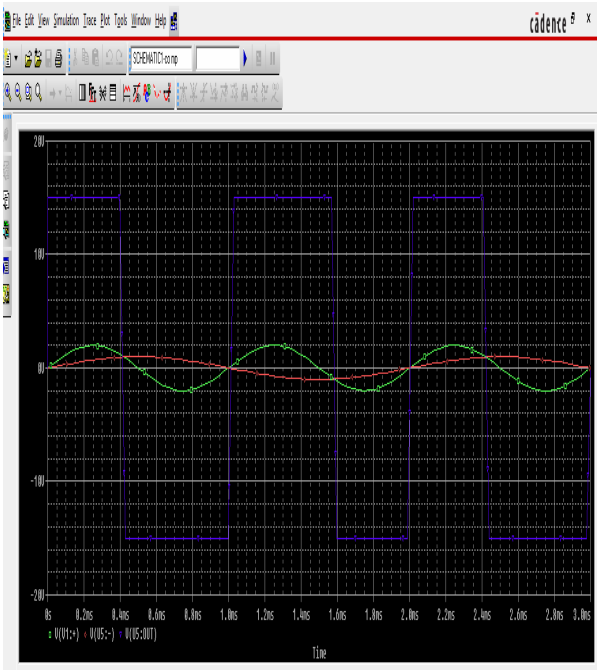

Fig.6.output of comparator

B.ADC Output Waveform

As shown in the Fig. 7 *&* *8*, as the input signal's amplitude increases the output signal in digital format also increses.Here output is swing from 0v to 1.3v.

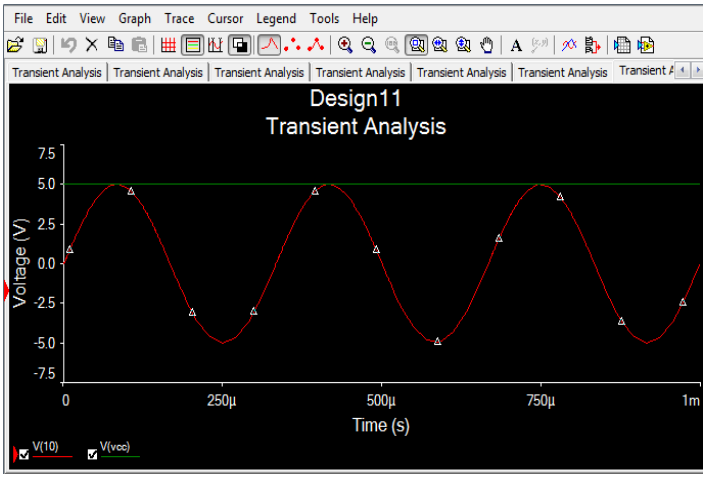

Fig.7. input of flash ADC

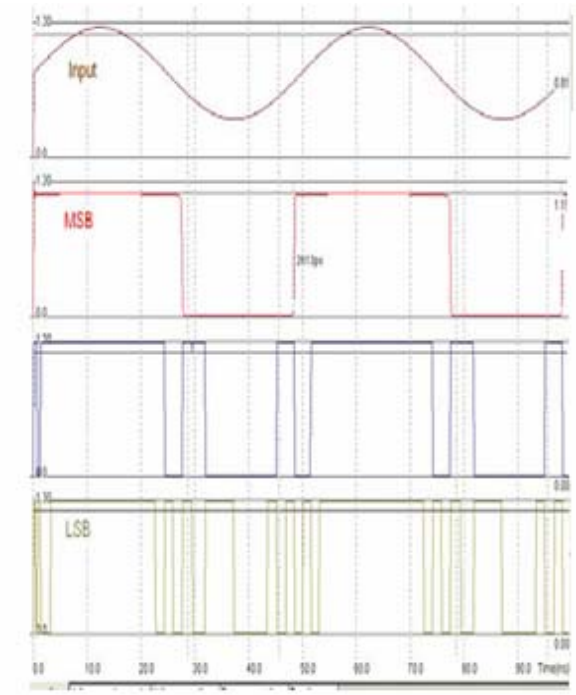

Fig. 8. Output of flash ADC

The 3-bit ADC based on flash type is designed in standard CMOS 0.18 um technology and the simulations are done by using Pspice.

C. Thermometer to Binary Encoder

An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another. The purpose of encoder is standardization, speed, secrecy, security, or saving space by shrinking size. Encoders are combinational logic circuits and they are exactly opposite of decoders. They accept one or more inputs and generate a multiple bit output code. Encoders perform exactly reverse operation than decoder. The simple block diagram and logic diagram of an encoder is given by fig.9 and fig.10.

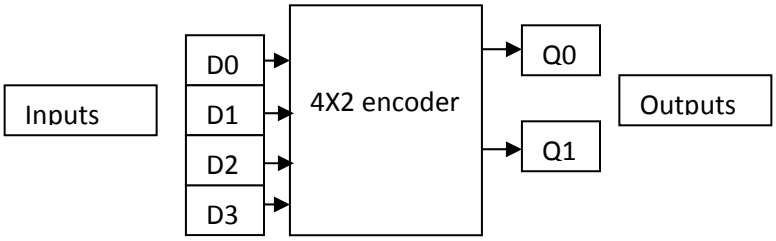

Fig.9.Block Diagram of 4 to 2 encoder

Below table 1 shows the two digital codes.

Inputs				Outputs	
D3	D2	D1	D0	Q1	Q0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	X	X

Table .1.TRUTH TABLE FOR THERMOMETER TO BINARY

This table can be used to design a suitable combinational circuit as Fig.9.

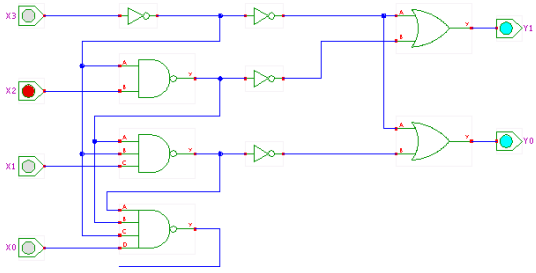

Fig.10. 4 to 2 encoder circuit diagram

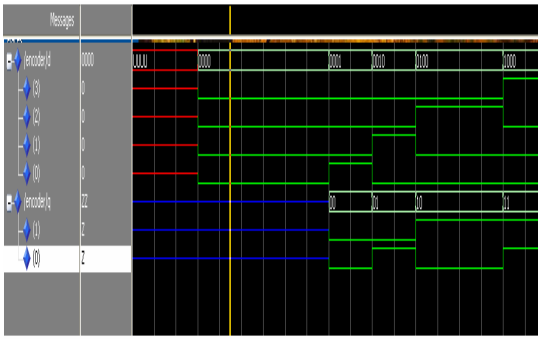

Fig.11.output of an encoder circuit

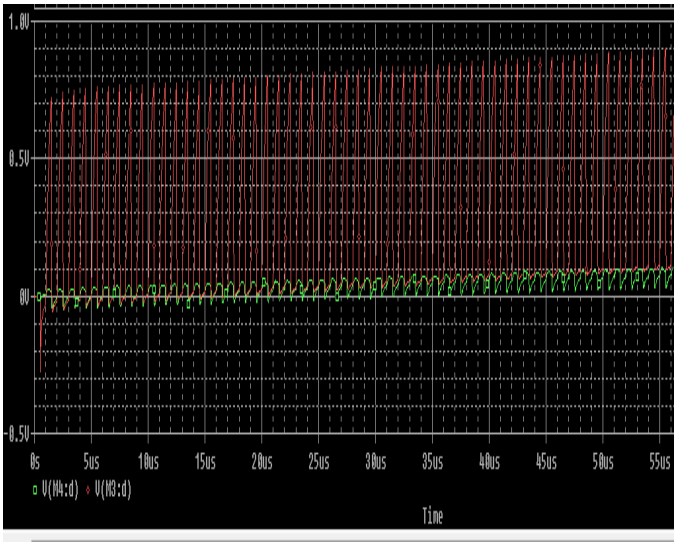

Fig.11.output of track/hold circuit.

Performances of the A/D converter using the proposed technique are confirmed by PSPICE simulations. A set of 0.18μm BSIM3v3 CMOS parameters is used for the simulations. Fig.12. shows the power consumption of the conventional flash A/D converter and the A/D converter based on the proposed technique at the maximum input frequency. The power consumption of the conventional A/D converter is 213 mW [7], on the other hand, the proposed T/H circuit is suppressed to 144 mV. This is 66 % of the conventional A/D converter's value. The number of comparators and their power consumption is drastically reduced and a reduction of input capacitor of the comparators brings reduction of the power consumption in the all previous stages, for example, the power consumption at an output buffer of T/H circuit and switches can be half. This low-power technique can reduce its power consumption as well as its chip area. This is one of the very important advantages over the conventional low-power technique. It is also confirmed that the A/D converter using the proposed technique shows almost the same DNL and INL characteristics.

V.COMPARISION CHART FOR EXISTING AND PROPOSED METHOD

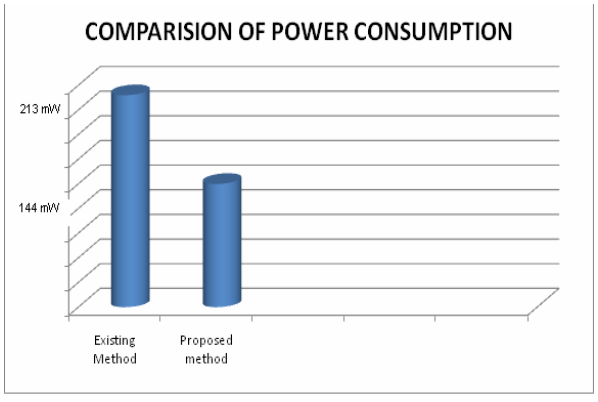

Fig.12.comparision of power consumption

The power consumption of the existing flash A/D converter is 213 mW, on the other hand the proposed flash A/D converter is suppressed to 144 mV.

VI. CONCLUSION:

This paper proposes a low-power design technique for flash analog-to-digital converters. The proposed technique reduces the power consumption of flash A/D converters by reducing the number of comparators. Flash A/D converters based on the proposed low-power technique consist of only 2^{N-1} + 1 comparators. On the other hand a conventional *N*-bit flash converter requires 2^N – 1 comparators. The proposed technique ideally can reduce more than 50% of the power required for the comparators.

VII. **Future Work**

The problem of flash ADCs lies with limited resolution, and high power dissipation because of the large number of high speed comparator. The ADC design can be used for low power and high speed applications. The proposed architecture is suitable for only balanced input signals. To overcome this drawback either TIQ comparators or dynamic comparators can be used.

VIII. REFERENCES

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