Simulation of Floating Gate MOSFET Using Silvaco TCAD Tools

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Abstract- *In today's increasingly mobile world, we are demanding more computational capacity than ever before and expect it to be available anytime in the palm of our hands. Integrated-circuit processes are reducing power requirements, and advancements in battery technology are being made; however, low-power analog systems still require orders of magnitude less power than comparable digital systems. Analog and mixed-signal systems offer tremendous computational capacity at very little cost in terms of power.*

One major weakness in analog integrated circuits is inaccuracies in the manufacturing process, which is manifested in device mismatch. Floating-gate transistors, because of their programmability, are an effective solution to this problem .The ability to store an initial charge on the floating gate allows fabrication imperfections to be corrected for devices that are required to be precisely matched, such as the input transistors of a deferential pair or a current mirror

I. INTRODUCTION

In today's increasingly mobile world, we are demanding more computational capacity than ever before and expect it to be available anytime in the palm of our hands. Integrated-circuit processes are reducing power requirements, and advancements in battery technology are being made; however, low-power analog systems still require orders of magnitude less power than comparable digital systems. Analog and mixed-signal systems offer tremendous computational capacity at very little cost in terms of power.

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II. STRUCTURE

An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and are electrically isolated from it. These inputs are only capacitive connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node.

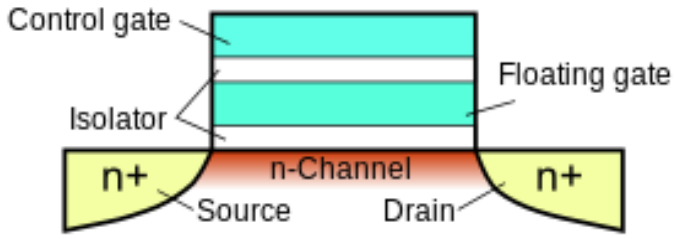


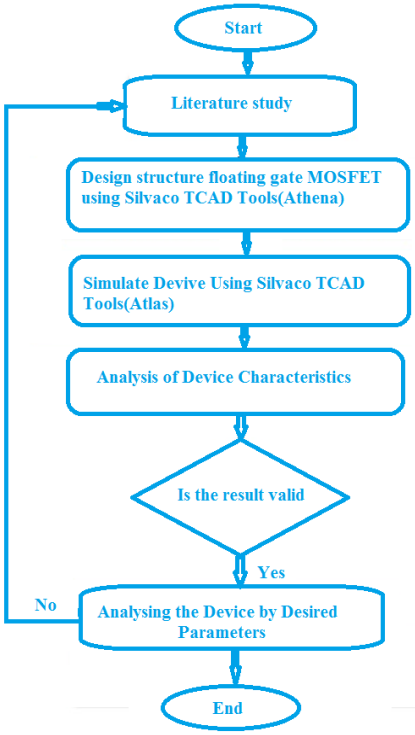
Figure 1: Structure of Floating gate mosfet

For applications where the charge of the FG needs to be modified, a pair of small extra transistors is added to each FGMOS transistor to conduct the injection and tunnelling operations. The gates of every transistor are connected together; the tunnelling transistor has its source, drain and bulk terminals interconnected to create a capacitive tunnelling structure. The injection transistor is connected normally and specific voltages are applied to create hot carriers that are then injected via an electric field into the floating gate

FGMOS transistor for purely capacitive use can be fabricated on N or P versions. For charge modification applications, the tunnelling transistor (and therefore the operating FGMOS) needs to be embedded into a well, hence the technology dictates the type of FGMOS that can be fabricated.

III. SIMULATION

A. The Simulations Steps



B. Simulations Result

The electrical performance of the device was performed by changing the desired parameters in the Silvaco TCAD Atlas file. The analysis is done by using Silvaco Tony plot where the graph will be analyzed to get the desired parameters. The data of parameters taken from the Silvaco Tony plot will be plot using Microsoft Excel Tools.

IV. DEVICE STRUCTURE

Figure shows the cross section of device structure of Floating Gate MOSFETs using Silvaco TCAD Athena

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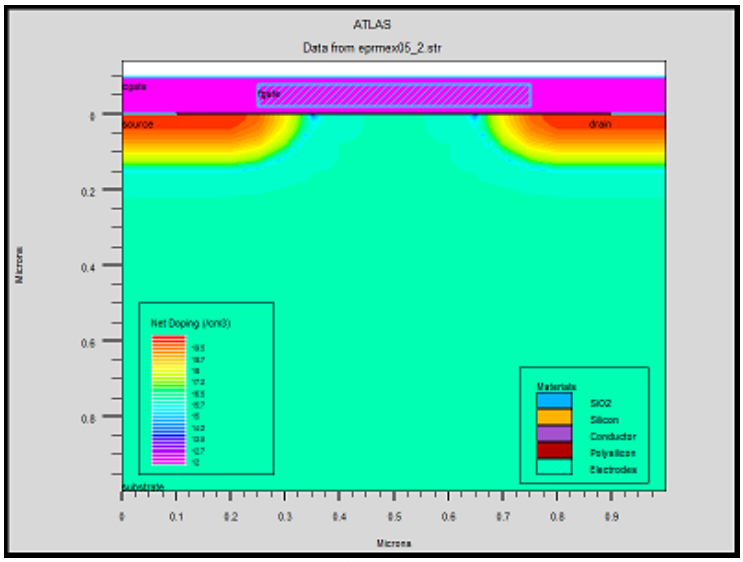

Figure2: The cross sectional structure of Floating Gate MOSFETs using Silvaco TCAD Athena

V. CHARACTERISTICS

Figure shows the output characteristic (I-V curve). The graphs have been obtained which is ID VS VGS.

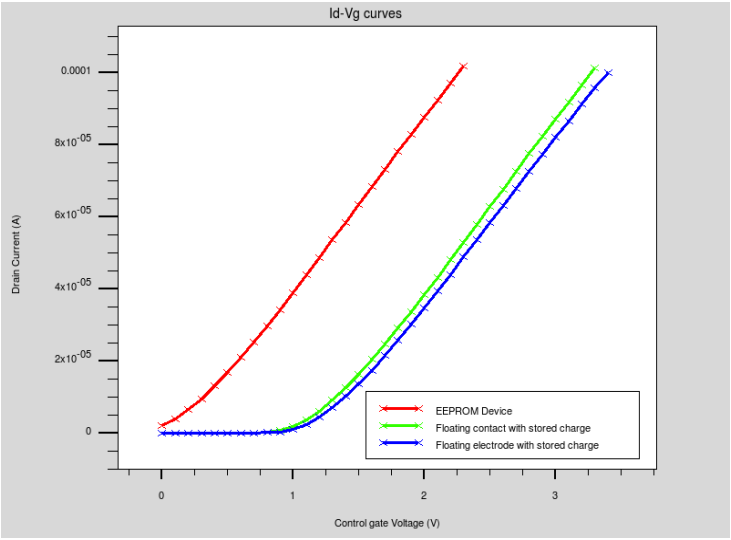

Figure 3: Graph of I_{DS} Vs V_{GS}

The threshold voltages for the three curves can be obtained from the results final file.

VI. CONCLUSION

This example creates a simple EEPROM cell with a polysilicon floating gate. It then highlights the difference between treating this as a floating contact (perfect conductor) or a floating electrode (semiconductor). It demonstrates

- Single gate EEPROM structure formation in Atlas.
- Mesh refinement in Atlas.
- Threshold voltage simulation before charging of polysilicon.
- Assignment of a charge to perfectly conducting contact.
- Threshold voltage simulation after charging.
- Assignment of a charge to a semiconductor contact.
- Threshold voltage simulation after charging.

The **FLOATING** parameter on the **CONTACT** statement causes the specified electrode to be treated as a perfect conductor, and therefore as an equipotential. Any stored charge is assumed to be evenly distributed and coupled to the device potential by using Gauss's flux theorem. For a polysilicon electrode this can be an imperfect approximation, because in the isolated semiconductor the potential and charge distributions will be position dependent in order to maintain the condition of zero steady state current flow. The **FLOATING** parameter on the **ELECTRODE** statement allows to modelling the floating gate as a semiconductor.

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